WHAT IS CLAIMED IS:

1. A method for determining a common write delay time of a memory in a computer system, comprising a north bridge chipset and a BIOS (Basic Input/Output System), said method comprising the steps of:

enabling said north bridge chipset to determine a write delay time;

issuing a write command from said north bridge chipset to said memory for writing a pattern to said memory;

writing said pattern to said memory according to said write command after said write delay time elapsed;

enabling said BIOS to read said pattern stored in said memory; and

enabling said BIOS to check whether said read pattern meets said written pattern, wherein said write delay time is passed if yes, and finally determining said common write delay time according to said write delay time.

2. The method according to claim 1, wherein said steps are executed repeatedly with different write delay times to find a write delay time range of said memory.

3. The method according to claim 2, wherein said computer system comprises a plurality of said memories, and said common write delay time is determined according to said write delay time ranges of said memories.

4. The method according to claim 3, wherein said common write delay time is an intersection set of said write delay time ranges.

5. A method for determining a common write delay time of plural ranks of memories in a computer system, said computer system comprising a north bridge chipset and a BIOS (Basic Input/Output System), said method comprising the steps of:

(a) selecting one of said ranks of memories;

(b) writing a pattern into said selected rank of memory according to different plurality of write delay times, comprising :

selecting one of said write delay times;

issuing a write command to said rank of memory for writing said pattern into one block of said memory; and

writing said pattern into said corresponding block according to

said write command after said selected write delay time has elapsed;

(c) repeating steps (a) and (b) to write said pattern into said ranks of memories according to said write delay times; and

(d) enabling said BIOS to read said pattern stored in said ranks of memories, determining a write delay time range of each rank of memories according to correctness of said read pattern, and then determine said common write delay time.

6. The method according to claim 5, wherein said common write delay time in step (d) is determined according to an intersection set of said write delay time ranges.

7. An apparatus for determining a common write delay time of a memory, comprising:

a CPU;

a north bridge chipset electrically connected to said CPU and said memory, said north bridge chipset writing a pattern into said memory according to different plurality of write delay times;

a south bridge chipset electrically connected to said north bridge

chipset; and

a BIOS (Basic Input/Output System) for reading said pattern stored in said memory and checking correctness of said read pattern to find a write delay time range of said memory and to determine said common write delay time.

8. The apparatus according to claim 7, further comprising a plurality of said memories.

9. The apparatus according to claim 8, wherein said BIOS reads said write delay time ranges of said memories, and then determines said common write delay time accordingly.

10. A method for determining a common write delay time of a memory in a computer system, said computer system comprising a north bridge chipset and a BIOS (Basic Input/Output System), said method comprising the steps of:

enabling said north bridge chipset to issue a write command to said memory so as to write a pattern to said memory according to a write delay time; and

enabling said BIOS to check whether said pattern stored in said memory meets said written pattern, wherein said write delay time is passed if yes, and said common write delay time is determined accordingly.

11. The method according to claim 10, wherein said two steps are repeatedly executed to find a write delay time range of each of said memories.

12. The method according to claim 11, wherein said computer system comprises a plurality of said memories, and said common write delay time is determined according to said write delay time ranges of said memories.

13. The method according to claim 12, wherein said common write delay time is determined according to an intersection set of said write delay time ranges.

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